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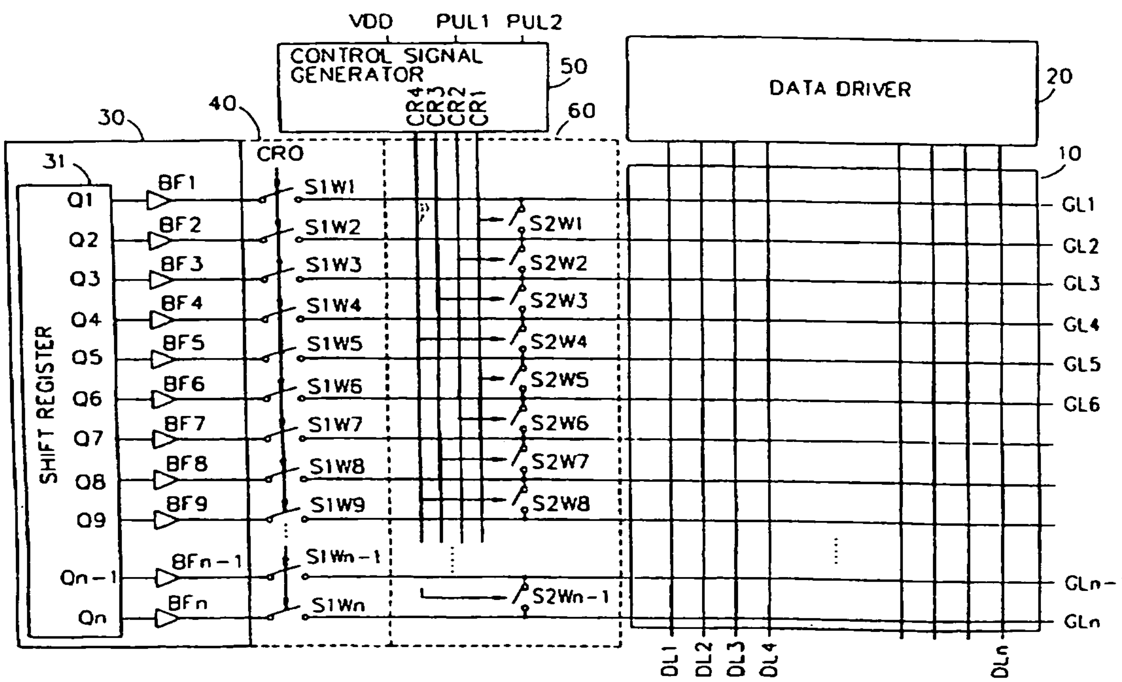
(54) Abstract Title
Gate driver circuit for LCD

(57) A low power gate driver circuit for a thin film transistor-liquid crystal display (TFT-LCD) has a switching device, positioned between each of the gate lines, and recycles the electric charge by discharging the electric charge which is stored in a capacitor of a gate line to a capacitor of another gate line, thereby reducing the power which the gate driver consumes.

FIG.3



GB 2 326 013 A

FIG. 1

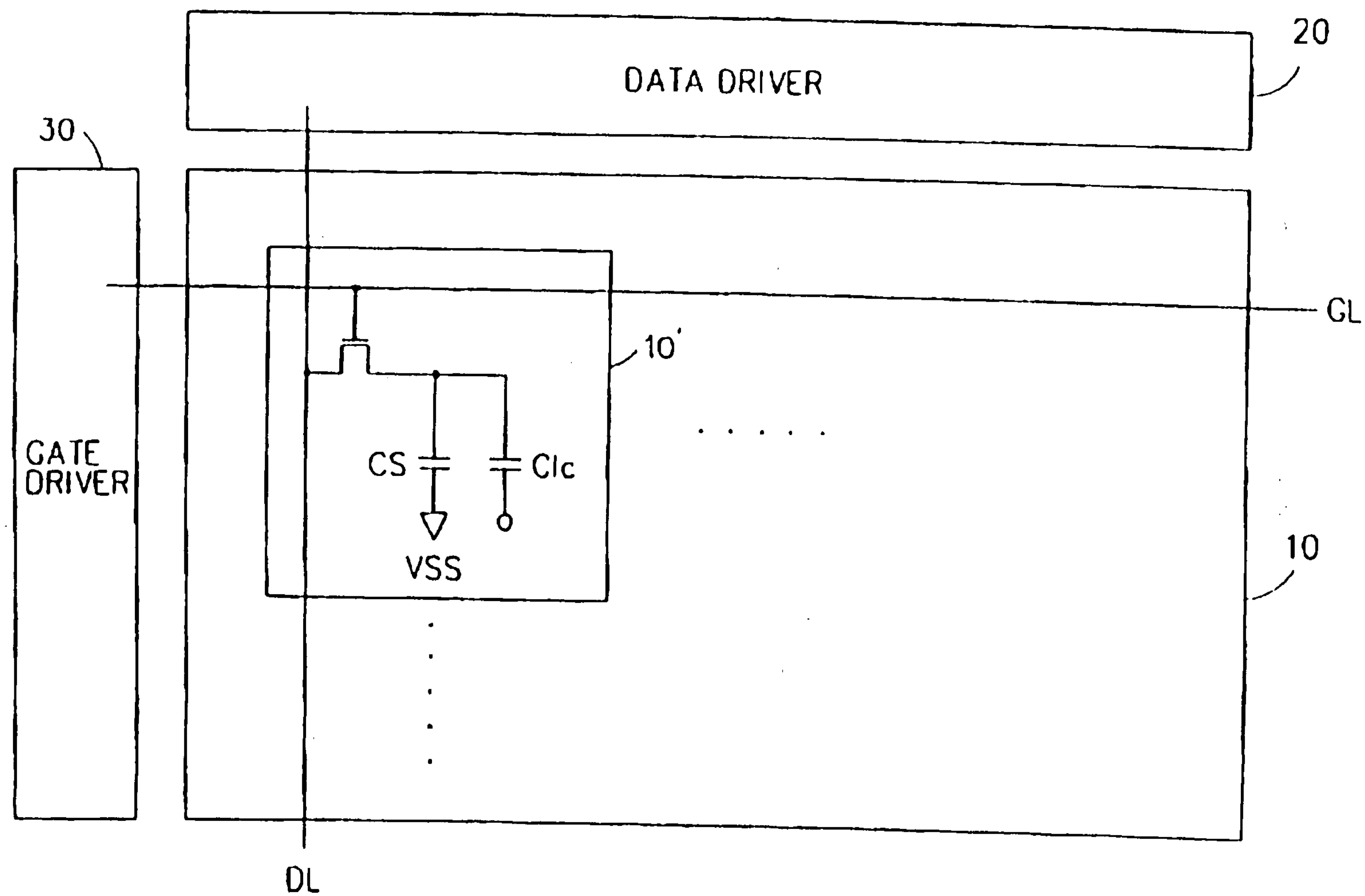


FIG. 2A

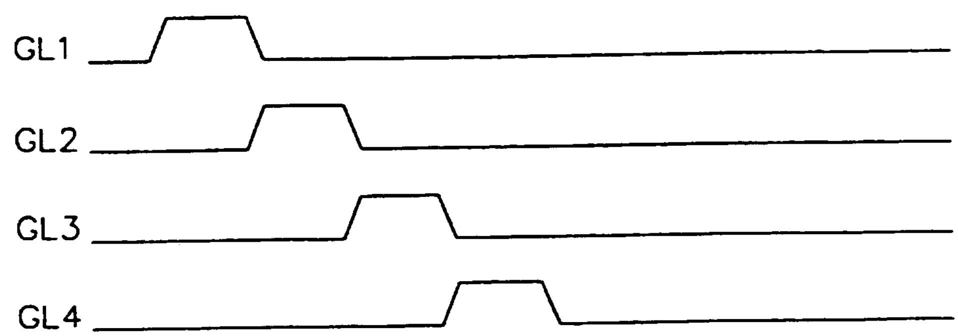


FIG. 2B

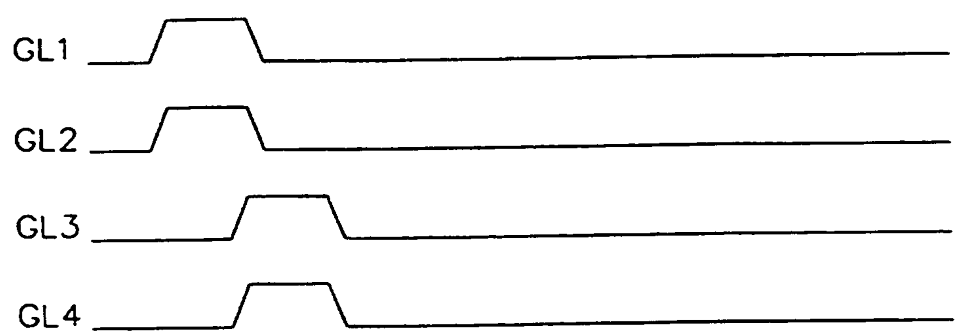


FIG. 2C

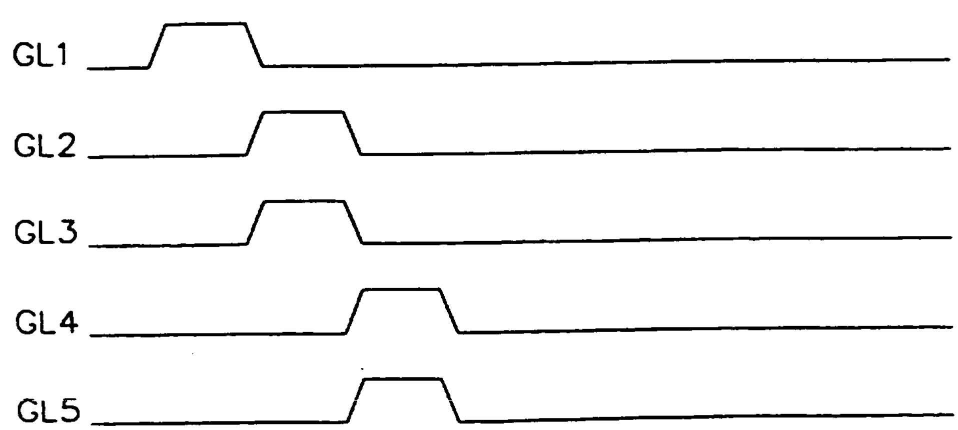
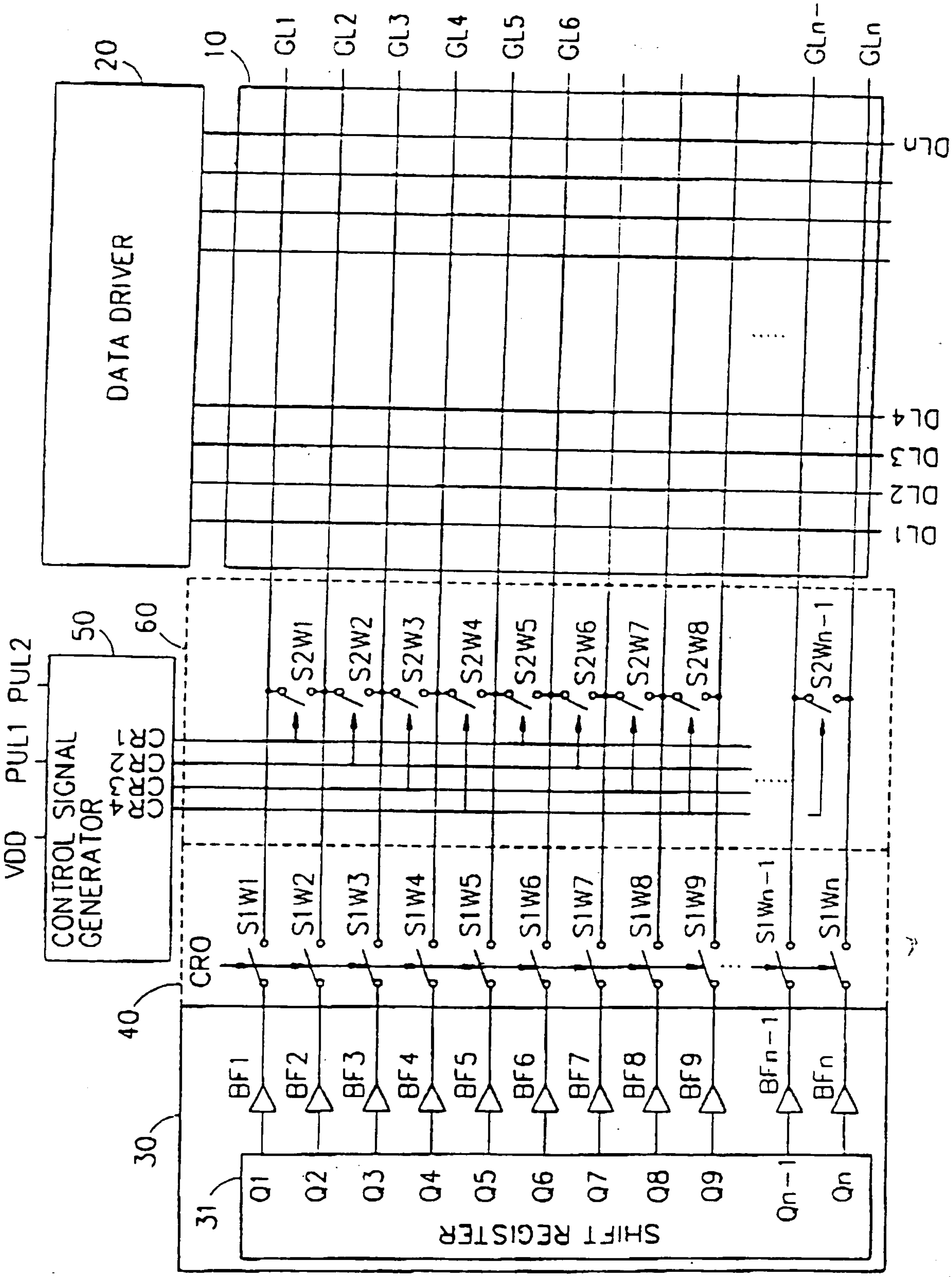


FIG.3



DATA DRIVER
CONTROL SIGNAL GENERATOR
SHIFT REGISTER
VDD
PUL1
PUL2
CR0
CR1
CR2
CR3
CR4
10
20
30
31
40
50
60
GL1
GL2
GL3
GL4
GL5
GL6
GLn-1
GLn
DL1
DL2
DL3
DL4
DLn
S1W1
S1W2
S1W3
S1W4
S1W5
S1W6
S1W7
S1W8
S1W9
S1Wn-1
S1Wn
S2W1
S2W2
S2W3
S2W4
S2W5
S2W6
S2W7
S2W8
S2Wn-1
BF1
BF2
BF3
BF4
BF5
BF6
BF7
BF8
BF9
BFn-1
BFn
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Qn-1
Qn

FIG. 4

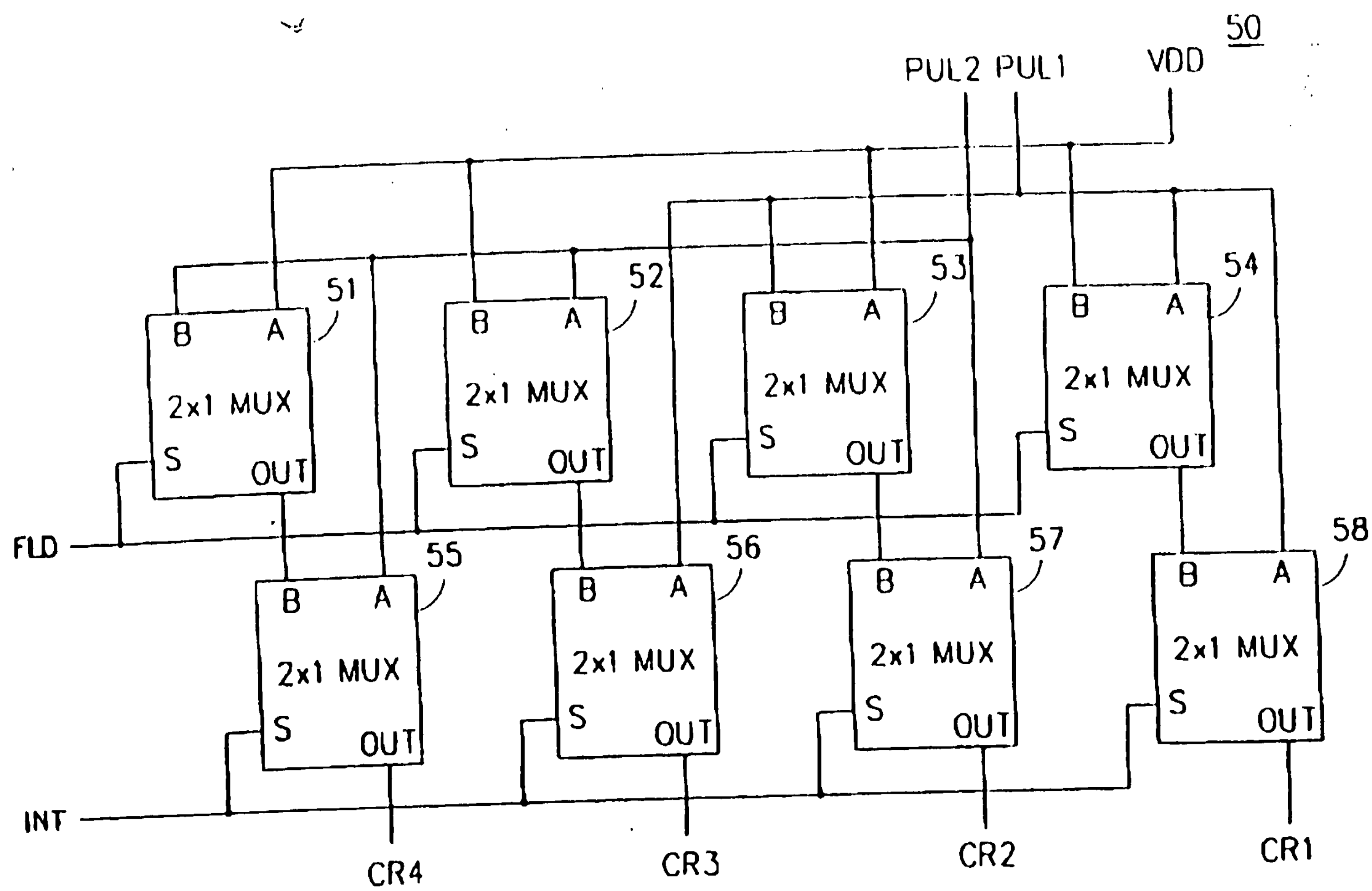

50
PUL2 PUL1
VDD
51
52
53
54
55
56
57
58
B
A
2x1 MUX
S
OUT
FLD
INT
CR4
CR3
CR2
CR1

FIG.5A

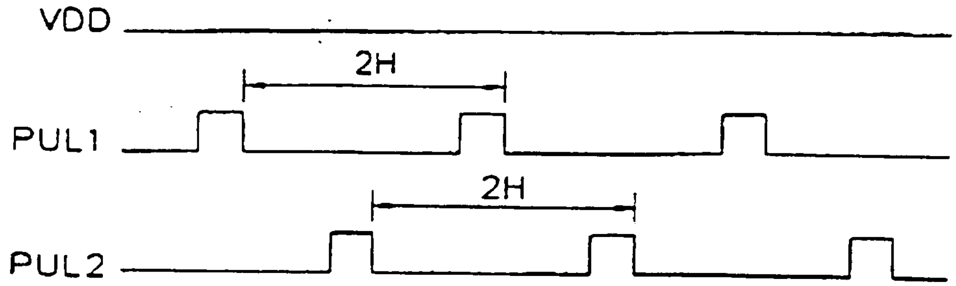


FIG.5B

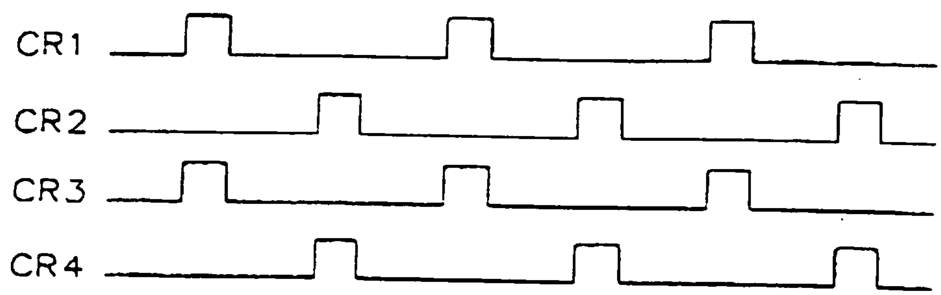


FIG.5C

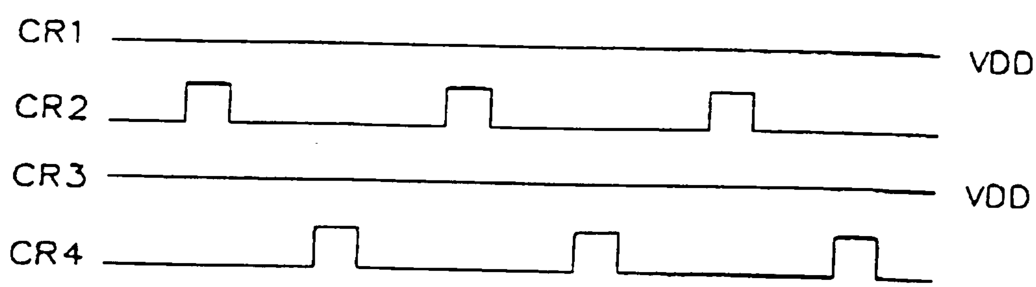


FIG.5D

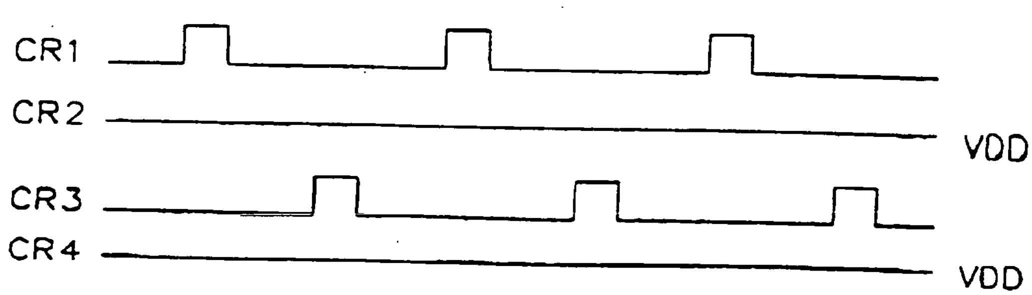


FIG.6A
FIG.6B
FIG.6C
FIG.6D
FIG.6E
FIG.6F
FIG.6G
FIG.6H
FIG.6I

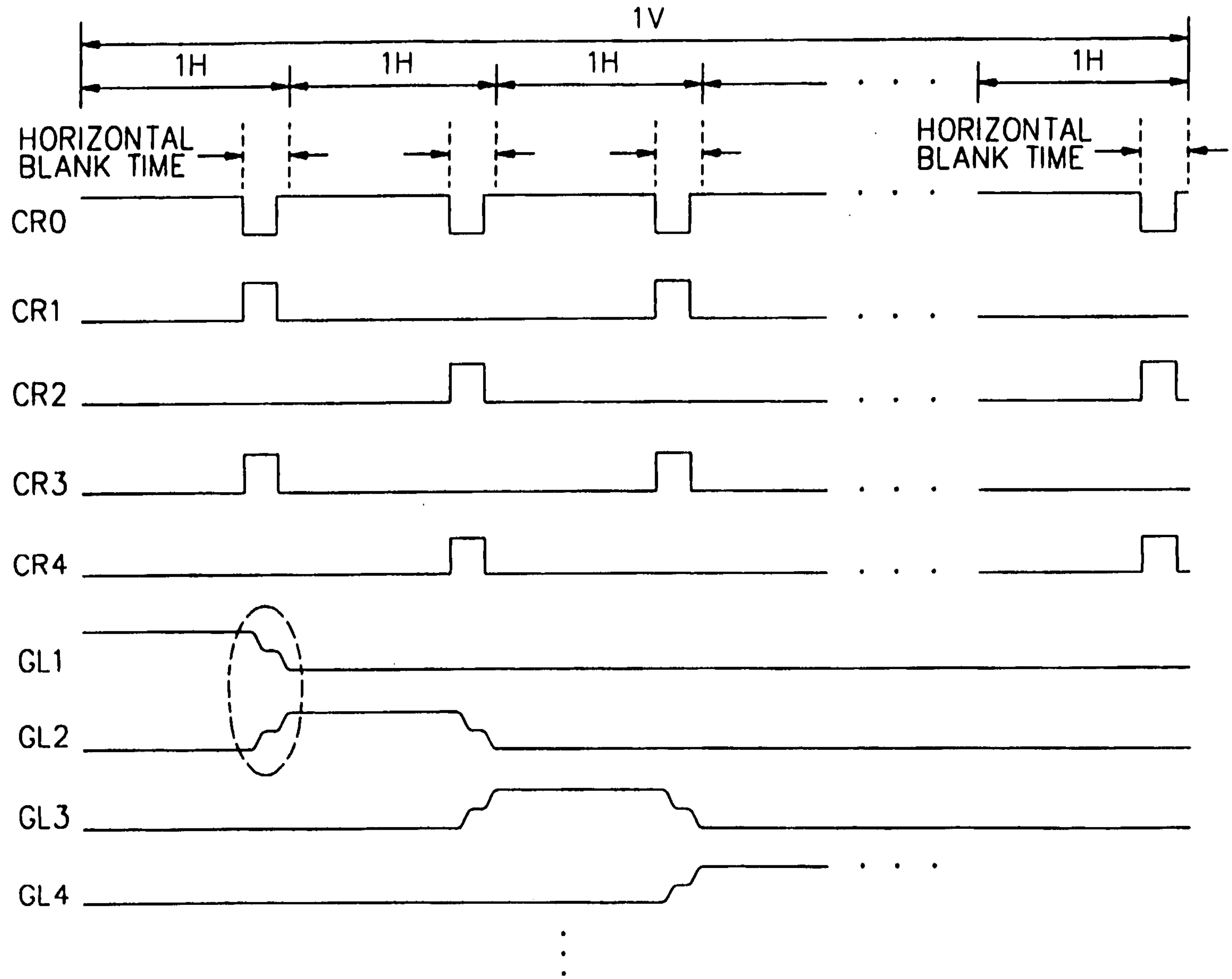


FIG.7

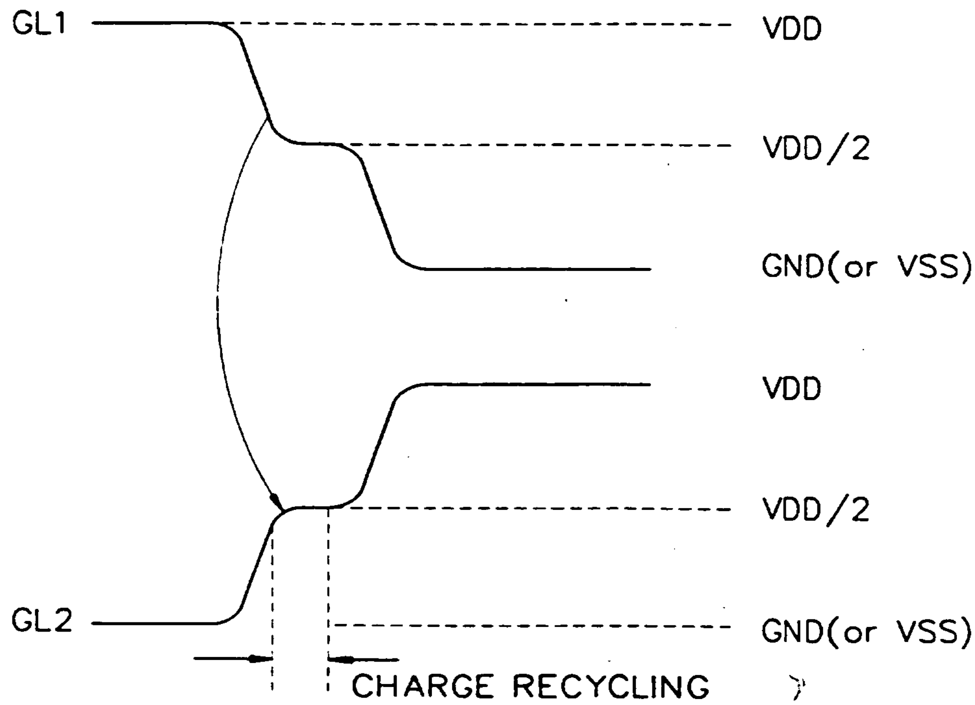

GL1
VDD
VDD/2
GND(or VSS)
VDD
VDD/2
GL2
GND(or VSS)
CHARGE RECYCLING

FIG.8A
FIG.8B
FIG.8C
FIG.8D
FIG.8E
FIG.8F
FIG.8G
FIG.8H
FIG.8I
FIG.8J
FIG.8K

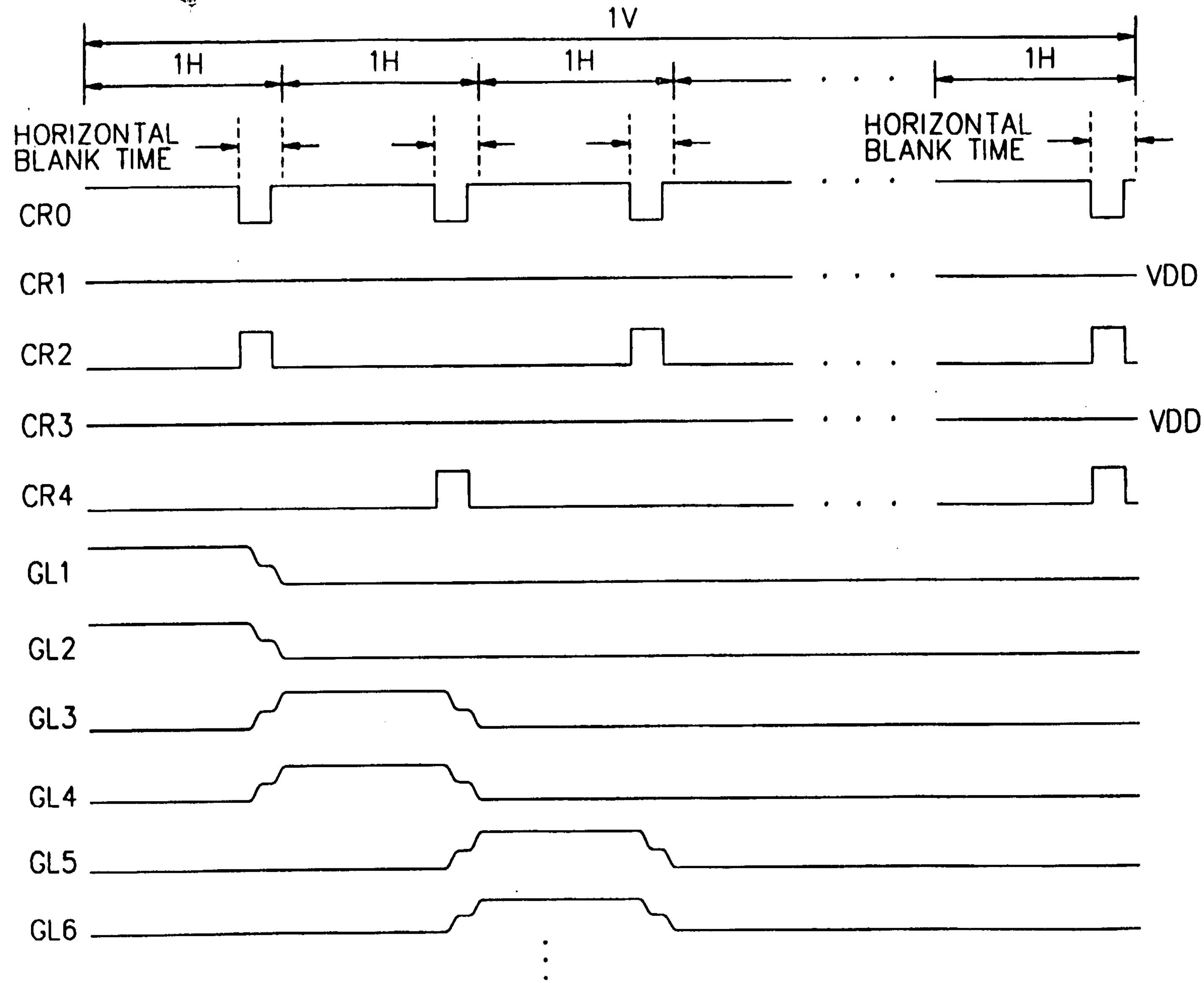


FIG.9A
FIG.9B
FIG.9C
FIG.9D
FIG.9E
FIG.9F
FIG.9G
FIG.9H
FIG.9I
FIG.9J
FIG.9K

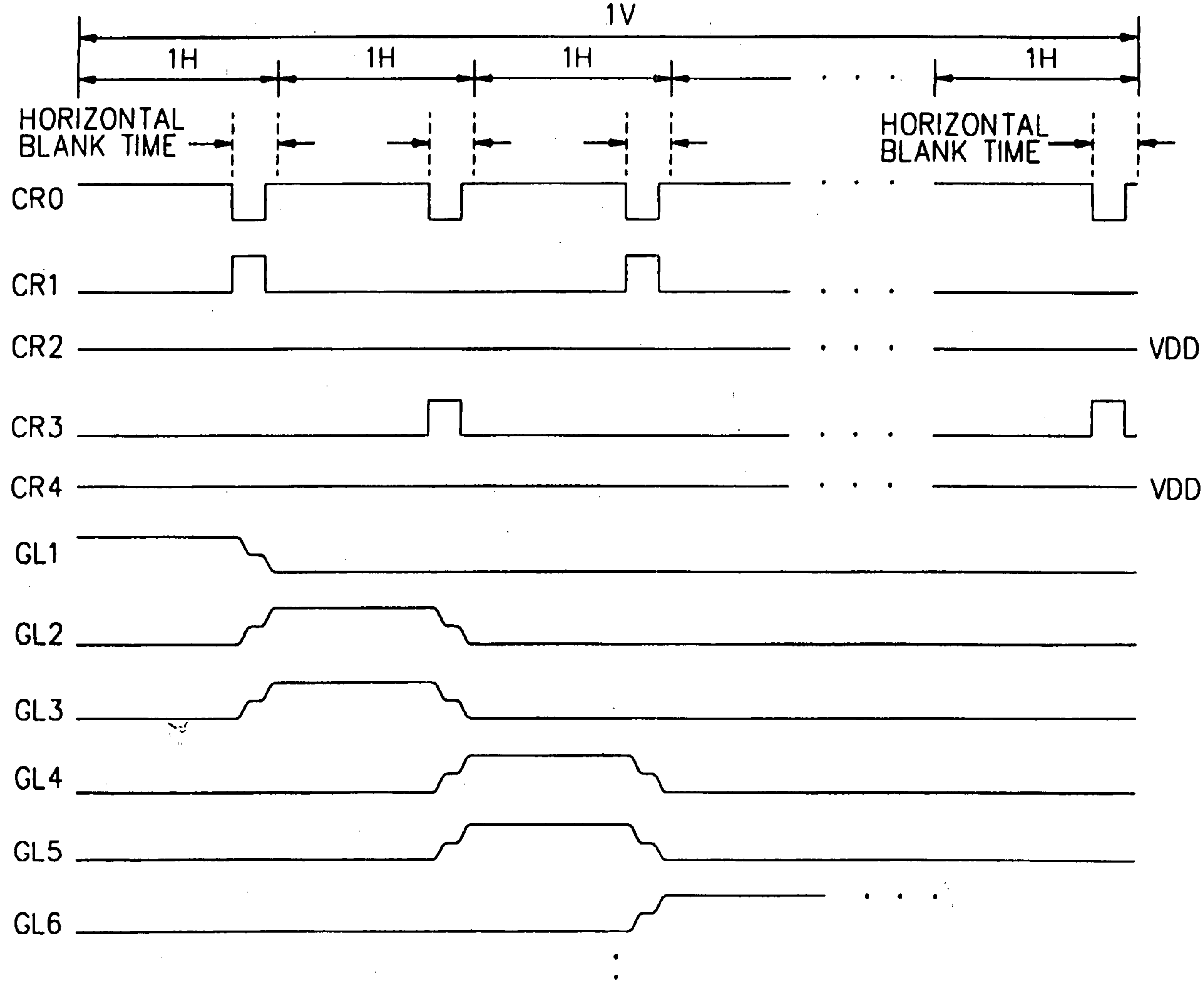


FIG.10

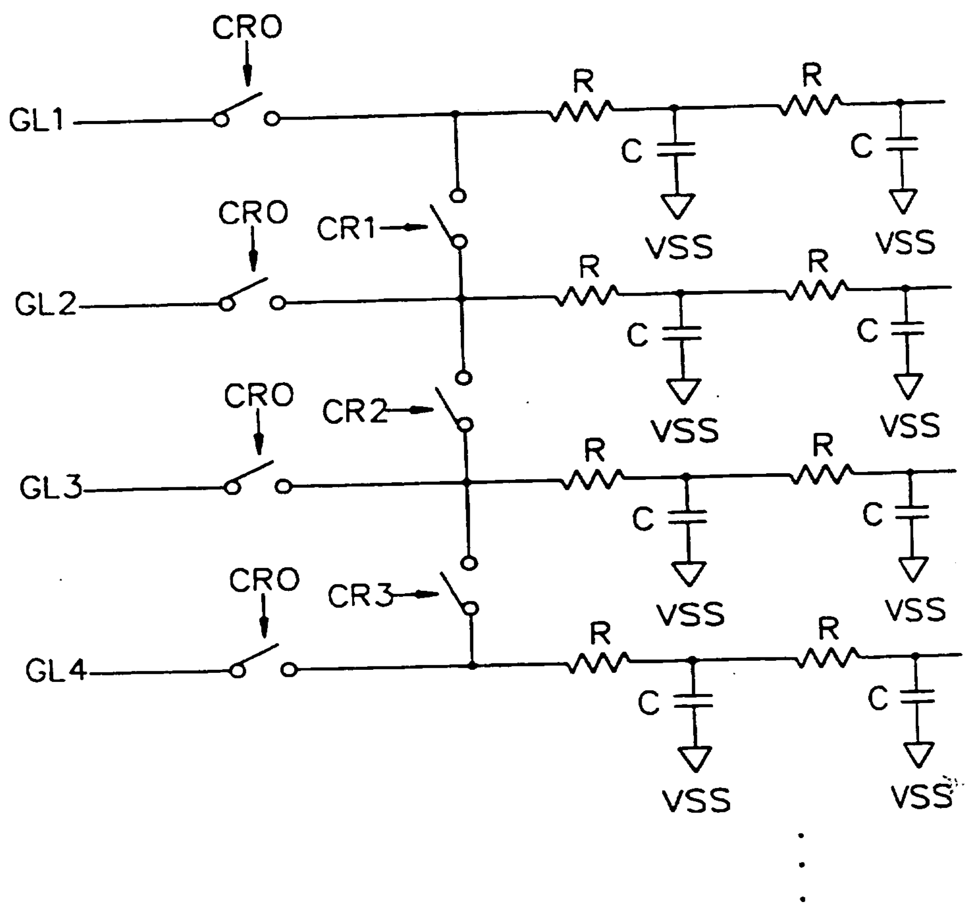

CRO
GL1
R
R
C
C
CRO
CR1
VSS
VSS
GL2
R
R
C
C
CRO
CR2
VSS
VSS
GL3
R
R
C
C
CRO
CR3
VSS
VSS
GL4
R
R
C
C
VSS
VSS

FIG. 11

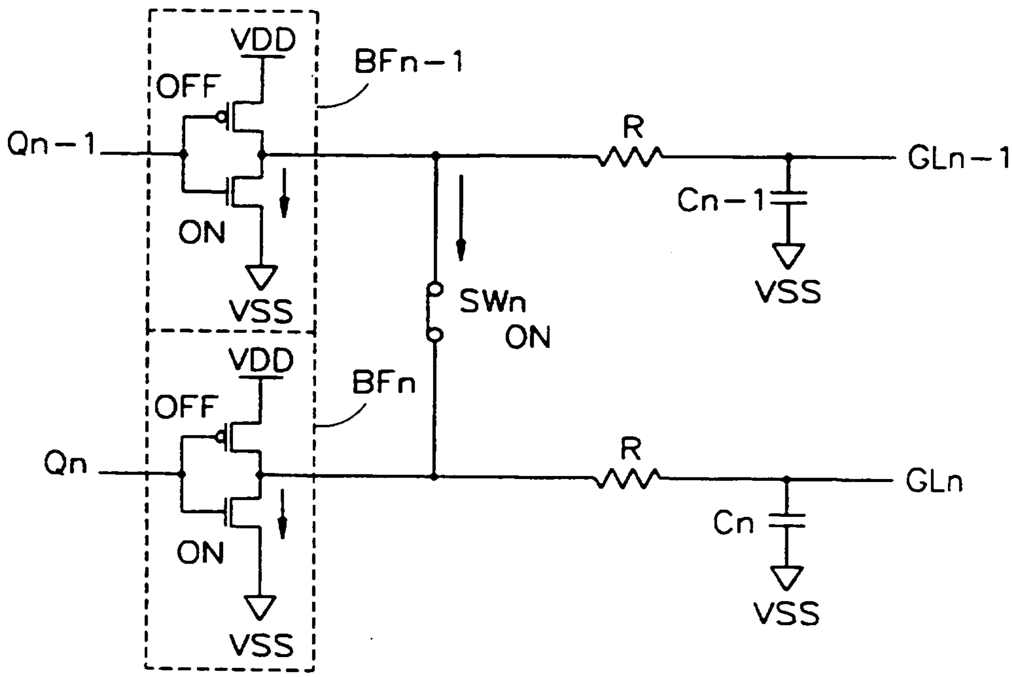
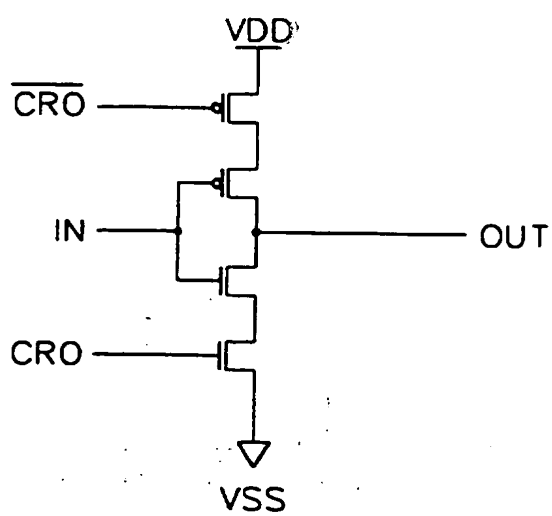

VDD
OFF
BFn-1
Qn-1
R
GLn-1
Cn-1
ON
SWn
VSS
ON
VDD
BFn
OFF
R
Qn
GLn
Cn
ON
VSS
VSS
VSS

FIG. 12


VDD
$\overline{CRO}$
IN
OUT
CRO
VSS

GATE DRIVER CIRCUIT FOR THIN FILM TRANSISTOR-LIQUID CRYSTAL DISPLAY (TFT-LCD)

The present invention relates to a thin film transistor-liquid crystal display (TFT-LCD), and in particular to an improved gate driver circuit of the TFT-LCD, the circuit being capable of reducing the power consumption of a gate driving unit.

As shown in Figure 1, a conventional TFT-LCD includes: a liquid crystal panel 10 having a plurality of pixels 10' which are formed at each intersection of gate lines GL and data lines DL; a data driver 20 for outputting a video signal to the liquid crystal panel 10 through the data lines DL; and a gate driver 30 for displaying the pixels 10' by driving the gate lines GL in sequence.

The pixels 10' are each configured using a thin film transistor TFT, a storage capacitor Cs and a liquid crystal capacitor Clc, the capacitors being connected in parallel at the source terminal of each thin film transistor TFT. The operation of the conventional TFT-LCD will now be described.

Initially, a shift register (not shown) located within the data driver 20 sequentially receives video data by one pixel, and stores the video data corresponding to each of the data lines DL.

The gate driver 30 outputs a signal having the waveform shown in Figure 2A, thus sequentially driving each of the plurality of gate lines GL. For the purpose of analysis, the gate lines GL can be modelled by means of their resistance and capacitance.

The magnitude of the resistance and capacitance varies depending on the screen size and the constituent material of the gate lines. In general the resistance may range from a few kΩ to tens of kΩ, and the capacitance may range from tens to hundreds of pF.

In office automation (O/A) applications, the gate driver 30 is configured to output a signal having the waveform shown in Figure 2A. Alternatively in audio video (A/V) applications, the gate driver 30 is configured to output a signal, in the case of an even number field (or frame) having the waveform shown in Figure 2B, or, in the case of an odd number field having the waveform shown in Figure 2C, thereby driving the gate lines GL.

In other words, in a so-called sequential scanning method for O/A applications, the gate driver 30 capacitively charges the gate lines GL, and discharges them to ground (or the supply rail VSS), in accordance with a signal having the pattern shown in Figure 2A, thereby driving the plurality of gate lines GL.

In the case of an even numbered field of a so-called double line simultaneous scanning method for A/V applications, as shown in Figure 2B, the gate driver 30 drives the plurality of gate lines GL by applying identical signals to the first and second gate lines GL1 and GL2, then applying identical signals to third and fourth gate lines GL3 and GL4, and so on for the remaining gate lines of the even numbered field.

In the case of the odd numbered field of the double line simultaneous scanning method (for the A/V application), as shown in Figure 2C, the gate driver 30 drives the plurality of gate lines GL by applying an initial signal to the first gate line GL1, and then applying identical signals to both the second and third gate lines GL2 and GL3, then applying identical signals to the fourth and fifth gate lines GL4 and GL5, and so on for the remaining gate lines of this field. Accordingly, the plurality of thin film transistors TFT connected to the selected gate lines GL are turned on, and video data stored in the shift registers (not shown) of the data driver 20 is applied to the thin film transistors, thereby displaying the video data on the liquid crystal panel 10. The above-described operation is successively repeated, and the video data is repeatedly displayed on the liquid crystal panel 10.

However, as a result of this operation, the output signal of the gate driver 30 swings from a VDD level to a VSS level (or ground), or from VSS (or ground) to VDD.

If the gate driver 30 drives an nth gate line GL, the power P_1 which the gate driver 30 consumes may be represented by the following formula (1):

$$P_1 = V_{DD.}\ I_{AV} = V_{DD.}\ (Cn.\ V_{SWING.}\ \text{Frame Frequency})\text{------------}(1)$$

where Cn is the capacitance of the nth gate line GL, I_{AV} is the average current, and V_{SWING} is the voltage swing of the scanning pulse.

Accordingly, in the conventional TFT-LCD driving circuit, the gate driver 30 outputs a signal which swings from VDD to VSS (or ground), or from VSS (or ground) to VDD in order to charge and discharge the capacitance of the gate line GL, thereby consuming power the amount of which is proportional to the value of VDD multiplied by V_{SWING}.

It is an object of the present invention to provide a driver circuit for a TFT-LCD which reduces power consumption.

According to the invention, there is provided a display device comprising: a plurality of first signal lines in a first direction; a plurality of second signal lines in a second direction; a display unit having a plurality of pixels, each pixel coupled to a corresponding first signal line and a corresponding second signal line; a switching device coupled to the said plurality of second signal lines; a control signal generator coupled to the switching device; a first driver coupled to the said plurality of first signal lines; and a second driver coupled to the switching device; wherein the switching device disconnects the said plurality of first second signal lines for a prescribed period of time to allow transfer of charges between corresponding second signal lines.

The display device may comprise a TFT-LCD low power gate driver circuit which uses switching devices connected between gate lines of the TFT-LCD to recycle electric charge by discharging the electric charge which is a charged capacitively charged on a plurality of the gate lines to be capacitively charged onto remaining gate lines, thereby to reduce the power which the gate driver circuit consumes.

The present invention will now be described by way of example with reference to drawings in which :-

Figure 1 is a block diagram of a conventional TFT-LCD;

Figures 2A to 2C are waveform diagrams showing output signals of the conventional gate driver in Figure 1;

Figure 3 is a block diagram of a TFT-LCD including a low power gate driver circuit in accordance with the invention, using an electric charge recycling technique ;

Figure 4 is a detailed circuit diagram of the control signal generator of Figure 3;

Figures 5A to 5D are waveform diagrams showing input and output signals of the control signal generator of Figure 4.

Figures 6A to 6I are waveform diagrams showing output signals of the gate driver, output signals of the control signal generator and electric charge recycling signals in a sequential scanning method for O/A applications;

Figure 7 is an enlargement of the recycling waveforms of Figures 6F and 6G;

Figures 8A to 8K are waveform diagrams showing output signals of the gate driver, output signals of the control signal generator and electric charge recycling signals, in an even numbered field of a double line simultaneous scanning method for A/V applications;

Figures 9A to 9K are waveform diagrams showing output signals of the gate driver, output signals of the control signal generator and electric charge recycling signals, in an odd numbered field of a double line simultaneous scanning method for A/V applications;

Figure 10 is an equivalent circuit diagram of a plurality of gate lines, and associated first and second switching units shown in Figure 3;

Figure 11 is a circuit diagram showing the operation of the switching units ; and

Figure 12 is a circuit diagram of a tri-state buffer which can be substituted for the combination of the switches of the first switching unit and the buffers of the gate driver in the circuit of Figure 3.

Referring to Figure 3, a low power gate driver circuit of the TFT-LCD using an electric charge recycling technique in accordance with the invention takes the form of a modification of the arrangement described above with reference to Figure 1. The arrangement of Figure 3 further includes: a first switching unit 40, positioned between the gate driver 30 and the liquid crystal panel 10, for holding a plurality of gate lines GL in a floating state in accordance with a control signal CR0 applied during a horizontal blank time interval; a control signal generator 50 for receiving a source or supply voltage VDD and first and second pulse signals PULl and PUL2, thereby to output a plurality of control signals CR1,...,CRy in accordance with the received input signals, where y is 4, regardless of the number of gate lines GLn, or, in the case of the control signals being directly applied to the second switching unit 60, y is n-1; and a second switching unit 60 for recycling the electric charge which is stored in the gate lines GL in accordance with the control signals CR1,...CRy.

The second switching unit 60 is located between the first switching unit 40 and the liquid crystal panel 10. Within the second switching unit 60, each of the gate lines GL are provided with a plurality of switches S2W1-S2Wn which connect the adjacent gate lines GL to each other in accordance with the control signals CR1,...,CRy outputted from the

control signal generator 50. The switches S2W1-S2Wn may be switching devices such as transmission gates or pass- transistors.

Note that the combination of both the plurality of buffers BF1-BFn (which are located within the gate driver 30), and the first switching unit 40, can be substituted by a tri-state buffer as shown in Figure 12..

Referring to Figure 4, the control signal generator 50 includes a plurality of multiplexers 51 to 58. Of these multiplexers, two of them, 51 and 52, selectively output either the second pulse signal PUL2 or the supply voltage VDD in accordance with an input selection signal FLD. A further two multiplexers 53 and 54 selectively output the first pulse signal PULl or the supply voltage VDD in accordance with the input selection signal FLD. Another multiplexer 55 outputs a signal which is either the output signal from multiplexer 51 or the second pulse signal PUL2 in accordance with a second input selection signal INT, and yet another multiplexer 56 outputs a signal which is either the output signal from the multiplexer 52 or the first pulse signal PULl in accordance with the input selection signal INT. A further multiplexer 57 output a signal which is either the output signal from the multiplexer 53 or the second pulse signal PUL2 in accordance with the second input selection signal INT, and yet a further multiplexer 58 outputs a signal which is either the output signal from the multiplexer 54 or the first pulse signal PULl in accordance with the second input selection signal INT. The output signals from multiplexers 55,56, 57 and 58 provide the respective control signals CR4, CR3, CR2 and CR1.

The operation of the above-described low power gate driver circuit will now be described.

A blank time interval exists between the display of successive frames during which time interval the video signal is externally inputted. A further blank time interval exists between the pulsing of successive gate lines GL, during which the video signal is not inputted thereto. The blank time interval between the pulsing of successive gate lines GL is referred to as the horizontal blank time, with the blank time interval between the

display of successive frames being referred to as the vertical blank time. In general the horizontal blank time is approximately 5.72 μ seconds, and the vertical blank time is approximately 10 μ seconds.

In order to support the aforementioned sequential scanning method for O/A applications and the double line simultaneous scanning method for A/V applications, the control signal generator 50 of the low power gate driver circuit outputs the control signals CR1,..,CRy, having a predetermined pulse width for a predetermined portion of the horizontal blank time interval, to the second switching unit 60 thereby recycling the charge on each of the gate lines GL by turning on the switches S2Wl ,... ,S2Wn of the second switching unit 60 The low power gate driver according to the present invention may use a reduced number of input pins by using the control signal generator 50 shown in Figure 4. It is not, therefore, necessary to receive all the control signals CRl,..,CRy from an external source.

As in the conventional circuit, the data driver 20 sequentially receives video data pixel by pixel , and outputs video data corresponding to each of the plurality of data lines DL. The gate driver 30 outputs gate line selection signals. thereby sequentially selecting each of the plurality of gate lines GL to display the video data.

As shown in Figure 10, the gate lines GL can be modelled as a number of resistances and capacitances, wherein the resistances R usually range from 3.5 KΩ to 6.5 KΩ, and the capacitances C are usually about l00pF.

The control signal generator 50 receives an external supply voltage VDD and the pulse signals PULl and PUL2, the waveforms of which are shown in Figure 5A. The control signal generator also receives the multiplexer input selection signal INT and FLD. When the input signal INT is 1, the control signals, shown in Figure 5B are generated, for use with the sequential scanning method for O/A applications. The value of the input signal FLD makes no difference to the control signals when INT is 1. When the input signal INT is 0 and the input signal FLD is also 0, the control signal generator 50 generates control

signals for even numbered fields of the so-called double-line simultaneous scanning method for A/V applications. These control signals are shown in Figure 5C. Finally, when the input signal INT is 0 and the input signal FLD is 1, control signals for odd numbered fields of the so-called double line simultaneous scanning method for A/V applications are generated. These are shown in Figure 5D.

In other words, the input signal INT is used to select whether the liquid crystal panel 10 is to be used for A/V or for O/A applications. When the input signal INT is 1, the liquid crystal panel 10 is used for O/A applications, and when the input signal INT is 0, the panel 10 is used for A/V applications. The input signal FLD is a field signal which selects the control signals to be outputted according to whether the displayed field is odd or even numbered. When the input signal FLD is 0, the control signals corresponding to the even numbered fields of the double line simultaneous scanning method are outputted. When the input signal FLD is 1, the control signals corresponding to the odd numbered fields are outputted.

The operation of the gate driver circuit due to the generated control signals for the sequential scanning method for O/A applications will now be described.

Initially, when the plurality of switches S1W1-S1Wn of the first switching unit 40 are turned on in accordance with the high level control signal CR0, as shown in Figure 6A, the gate driver 30 outputs a gate line selection signal of a VDD level through the buffer BF1 of the output terminal, thus driving (charging) the capacitor of the first gate line GL1.

When the input signal INT is 1 (regardless of the value of FLD), the control signal generator 50 initially outputs control signal CR1 as shown in Figure 5B. This signal is outputted during the horizontal blank time , thereby turning on switch S2W1 of the second switching unit 60, as well as S2W5.

As a result, the charge on the first gate line GL1 is discharged to the capacitor of the second gate line GL2, the capacitor thus being raised to a VDD/2 level by recycling the charge and without receiving any charge from an external source (the gate driver). This operation is illustrated in Figures 6F and 6G, the charge recycling operation being shown in enlarged form in Figure 7.

Note that if the two switches S2W1 and S2W2 of the second switching unit 60 were to be simultaneously turned on after the second gate line GL2 is driven (charged), the electric charge on the capacitor of the second gate line GL2 would be transferred to the capacitors of both the third and first gate lines GL3 and GL1 . In order to avoid such a situation, control signals CR1 and CR3, which, as Figure 3 shows, control the odd numbered switches S2W1, S2W3 etc. of the second switching unit 60, and control signals CR2 and CR4, which control the even numbered switches S2W2, S2W4 etc. are alternately supplied thereto once every 2H (where H is a horizontal scanning cycle). Using this operation, no two adjacent switches in the second switching unit are switched on at the same time. The control signals are shown in Figures 6B to 6E.

The switches S1Wl ,...,S1Wn of the first switching unit 40 are turned off in accordance with the low level control signal CR0 at the time when the electric charge is being transferred between the gate lines GL. i.e. during the horizontal blank time.

If the switches S1Wl ,...,S1Wn of the first switching unit 40 were not present or the switches S1W1 ,...,S1Wn thereof were constantly held in a turned-on state as shown by way of example in Figure 11, the charge on capacitor Cn-l of gate line GLn-l would be completely discharged through the turned-on pull-down transistor in buffer BFn of the gate driver 30. Thus the electric potential of a capacitor Cn in a gate line GLn would not be raised to the VDD/2 level by the charge being transferred from the gate line GLn-1.

By using the switches S1W1,..., S1Wn of the first switching unit 40 the capacitor Cn of the gate line GLn may be completely charged by the buffer BFn of the gate driver 30, that is, charge supplied from the external supply VDD.

The operation of the gate driver circuit due to the generated control signals for the even numbered fields of the double line simultaneous scanning method for A/V applications will now be described.

As shown in Figure 2B, the gate driver 30 applies identical gate line selection signals to the first gate line GLl, and the second gate line GL2, and then applies identical signals to the third gate line GL3 and the fourth and fifth gate line GL4 and so on for the remaining gate lines.

As shown in Figures 8B to 8E, when both of the input signals INT and FLD are 0 so as to select the even numbered field mode, the control signal generator 50 outputs control signals CR (2k-1), (where k = 1, 2, 3.....n/2) at a VDD level so as to turn on the odd numbered switches S2W (2k-1), (where k = 1, 2, 3...... n/2) of the second switching unit 60 during the horizontal blank time interval. In addition pulse-type control signals CR (2k), (where k = 1, 2, 3......n-2/2) are alternated, as shown in Figures 8C and 8E, to turn on each even numbered switch S2W (2k), (where k = 1, 2, 3.....n-2/2) of the second switching unit 60 once every 2H. In accordance with this operation, recycling of the charge between adjacent gate lines GL is accomplished. As shown in Figures 8F to 8K, the first and second gate lines GLl and GL2, the third and fourth gate lines GL3 and GL4, and the fifth and sixth gate lines GL5 and GL6 are each of an identical electric potential, and the charge recycling is accomplished between the gate lines GL2n and gate lines GL2n+l(e.g. between gate lines 2 and 3, 4 and 5, etc.)

The operation of the gate driver circuit due to the generated control signals for the odd numbered fields of the double-line simultaneous scanning method for A/V applications will now be described.

As shown in Figure 2C, the gate driver 30 applies a turn-on signal to the first gate line GLl, then identical signals to the second and third gate lines GL2 and GL3, , and then identical signals to the fourth and fifth gate lines GL4 and GL5, and so on for the remaining gate lines.

As shown in Figures 9B to 9E, when the input signal INT is 0 and the input signal FLD is 1 (so as to select the odd numbered field mode) the control signal generator 50 turns on the even numbered switches S2W (2k), (where k = 1, 2, 3.....n-2/2) of the second switching unit 60 by applying the control signals CR (2k), (where k = 1,2,3.....n-2/2) at a VDD level, whilst alternately applying pulse-type control signals CR (2k-1), (where k = 1, 2, 3......n/2) to the odd numbered switches S2W (2k-1), (where k = 1, 2, 3......n/2) of the second switching unit 60 once every 2H during the horizontal blank time(as shown in Figures 9B and 9D). As shown in Figures 9F to 9K, the second and third gate lines GL2 and GL3, and the fourth and fifth gate lines GL4 and GL5 are each of an identical electric potential, and charge recycling is accomplished between the gate lines GL2n-1 and gate lines GL2n (e.g. between gate lines 1 and 2, 3 and 4, etc.).

In accordance with the above-described operation, whereas the output signal from the conventional gate driver 30 swings from a VDD level to a VSS level the output signal from the present gate driver 30 swings from a VSS (or ground) level to a VDD/2 level, or from a VDD/2 level to a VDD level. In this case, the electrical power P which the gate driver 30 consumes, is determined by the following formula (2):-

$$P_2 = V_{DD.} (C_n . V_{SWING} /2. \text{ Frame Frequency}) = P_1 /2\text{----------}(2)$$

where, Cn is the capacitance of the nth gate line GLn.

Accordingly, the power P_2 which is consumed by the gate driver 30 is decreased to be about 1/2 of the power P_1 consumed by the conventional gate driver.

It should be noted that the combination of both the switches S1W1 -S1Wn of the first switching unit 40 and the buffers BFn in the gate driver 30 can be substituted by a tri-state buffer as shown in Figure 12. Furthermore, the switching devices of the second switching unit 60 can be substituted by a plurality of transmission gates or pass-transistors.

In summary, as described above, the TFT-LCD driver circuit recycles the charge between gate lines by controlling switches connected between each of the gate lines during a horizontal blank time interval. The driver circuit is applicable to both a sequential scanning method and a double-line simultaneous scanning method.

The described circuit can reduce the power which the gate driver consumes to be about 1/2 of that consumed by the conventional gate driver This is achieved by controlling the transmission gates, which are connected between each of the gate lines, during the horizontal blank time interval.

In addition, since the gate driver is capable of operating with reduced power consumption, it will generate less heat. This means that if the liquid crystal display LCD is fabricated using poly-silicon thin film transistors (Poly-Si TFT), the properties of the liquid crystal display and TFTs are less likely to deteriorate due to the effects of heating.

CLAIMS

1. A display device comprising:

a plurality of first signal lines in a first direction;

a plurality of second signal lines in a second direction;

a display unit having a plurality of pixels, each pixel coupled to a corresponding first signal line and a corresponding second signal line;

a switching device coupled to the said plurality of second signal lines;

a control signal generator coupled to the switching device;

a first driver coupled to the said plurality of first signal lines; and

a second driver coupled to the switching device,

wherein the switching device disconnects the said plurality of first second signal lines for a prescribed period of time to allow transfer of charges between corresponding second signal lines.

2. A display device according to claim 1, wherein the display unit is a liquid crystal display panel.

3. A display device according to claim 2, wherein each pixel comprises a transistor having first and second electrodes and a control electrode, a first capacitor and a second capacitor, the first and second capacitors being coupled to the second electrode.

4. A display device according to claim 3, wherein the first driver is a data driving unit and the first signal lines are data lines, a corresponding data line being coupled to the first electrode of a corresponding transistor of the pixel.

5. A display device according to claim 4, wherein the second driver is a data driving unit and the second signal lines are gate lines, a corresponding gate line being coupled to the control electrode of the corresponding transistor of the pixel.

6. A display device according to any preceding claim, wherein the prescribed period of time occurs during horizontal blank times.

7. A display device according to any preceding claim, wherein the switching device comprises:

a first switching unit responsive to a first control signal for disconnecting the said plurality of second signal lines during the prescribed period of time;

a second switching unit responsive to a plurality of second control signals from the control signal generator to allow transfer of charges between corresponding second signal lines.

8. A display device according to claim 7, wherein the second driver comprises:

a shift register having a plurality of output terminals; and

a plurality of buffers coupled to the said plurality of output terminals.

9. A display device according to claim 8, wherein:-

the first switching unit includes a plurality of first switches coupled to the said plurality of buffers and responsive to the first control signal, and

the second switching unit includes a plurality of second switches, each of the said plurality of second switches being coupled between adjacent ones of the second signal lines and being responsive to a corresponding second control signal.

10. A display device according to claim 9, wherein each of the said plurality of first and second switches is a pass transistor or a transmission gate.

11. A display device according to claim 1, wherein the second driver comprises:

a shift register having a plurality of output terminals; and

a plurality of buffers coupled to the said plurality of output terminals.

12. A display device according to claim 7, wherein:-

the first switching unit comprises a plurality of tri-state buffers coupled to outputs of the second driver and the plurality of second signal lines, and

the second switching unit comprises a plurality of switches, each switch coupled between corresponding second signal lines and being responsive to a corresponding second control signal.

13. A display device according to any preceding claim, wherein the control signal generator comprises:-

a plurality of first multiplexers coupled for receiving externally applied control signals and responsive to a first input control signal;

a plurality of second multiplexers, each coupled for receiving a corresponding externally applied control signal and responsive to a second input control signal to output a corresponding second control signal.

14. A display device according to claim 13, wherein the first input control signal is indicative of a first or second mode of operation, and the second input control signal is indicative of a first or second operation associated with the second mode of operation.

15. A display device according to claim 14, wherein the first mode of operation corresponds to office automation application and the second mode of operation corresponds to audio/video application.

16. A display device according to claim 15, wherein the first operation associated with the second mode of operation is for an even number field for a double line simultaneous scanning method, and said second operation associated with the second mode of operation is for an odd number field for the double line simultaneous scanning method.

17. A gate driver circuit for use with a display panel, comprising:

a plurality of gate lines for the transmission of gating pulse signals in a predetermined sequence from a pulse signal source to the panel;

a plurality of controllable interconnecting devices coupled between the gate lines;

control means coupled to the interconnection devices in a predetermined sequence during a blanking interval to cause the devices to conduct for part of the blanking interval such that the change stored on a pulsed gate line is shared with a connected gate line during the blanking interval; and

gate line isolation means for isolating the gate lines from the pulse signal source whilst the gate lines are interconnected.

18. A driver circuit according to claim 17, wherein each of the interconnection devices is connected between a respective pair of gate lines.

19. A driver circuit according to claim 18, having a group of gate lines arranged in a parallel array, wherein each interconnection device interconnects a gate line in the array to the next adjacent gate line (i+1), the gate lines within the group being interconnected by (n-1) interconnection devices.

20. A driver circuit according to any of claims 17 to 19, wherein the isolation means comprise a plurality of switching devices coupled in series in the gate lines between the pulse signal source and the interconnected devices.

21. A display system comprising a thin film transistor liquid crystal display panel and a gate driver circuit according to any of claims 17 to 20 wherein the thin film transistor liquid crystal display comprises a plurality of thin film transistors arranged as a rectangular array forming rows and columns, the gate terminals of each row of transistors being electrically connected to a respective one of the gate lines; and a plurality of data lines for transmitting video data signals to the drain terminals of respective columns of transistors; the gating pulse signals cause

transfer of the data transmitted by the data lines to capacitive storage means for display.

22. A low power gate driver circuit of a thin film transistor-liquid crystal display(TFT-LCD) recycling an electric charge, which controls the switching device, positioned between each of gate lines, and recycles the electric charge by discharging the electric charge which is charged in a capacitor of a gate line to a capacitor of another gate line, thereby capable of reducing energy which a gate driver consumes.

23. A display device constructed and arranged substantially as herein described and shown in Figures 3 to 12 of the drawings.

24. A gate driver circuit constructed and arranged substantially as herein described and shown in Figures 3 to 12 of the drawings.

The Patent Office

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Application No: GB 9811665.0
Claims searched: 1 to 23

Examiner: Geoffrey Pitchman
Date of search: 30 September 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): G5C (CHB)

Int Cl (Ed.6): G09G3/36

Other: ONLINE: EDOC WPI JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2188473 A	(TOSHIBA)-see abstract	1
X	EP 0488516 A	(IBM)-see abstract	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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